International Rectifier

Applications
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Lead-Free

Ordering Information

<table>
<thead>
<tr>
<th>Base Part Number</th>
<th>Package Type</th>
<th>Standard Pack</th>
<th>Complete Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRFB7430PbF</td>
<td>TO-220</td>
<td>Tube</td>
<td>IRFB7430PbF</td>
</tr>
</tbody>
</table>
Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

Repetitive rating; pulse width limited by max. junction temperature.

Limited by \( T_{J,max} \) starting \( T_J = 25°C \), \( L = 0.15mH \)
\( R_G = 50Ω, I_{AS} = 100A, V_{GS} = 10V \).

\( I_{SD} \leq 100A, \frac{di}{dt} \leq 990A/μs, V_{DD} \leq V_{BRDSS}, T_J \leq 175°C \).

Notes:

1. Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
2. Repetitive rating; pulse width limited by max. junction temperature.
3. Limited by \( T_{J,max} \) starting \( T_J = 25°C \), \( L = 0.15mH \)
\( R_G = 50Ω, I_{AS} = 100A, V_{GS} = 10V \).
4. Pulse width \( \leq 400μs \); duty cycle \( \leq 2\% \).
5. \( C_{oss \, eff \, (TR)} \) is a fixed capacitance that gives the same charging time as \( C_{oss} \) while \( V_{DS} \) is rising from 0 to 80% \( V_{DSS} \).
6. \( C_{oss \, eff \, (ER)} \) is a fixed capacitance that gives the same energy as \( C_{oss} \) while \( V_{DS} \) is rising from 0 to 80% \( V_{DSS} \).
7. \( R_i \) is measured at \( T_J \) approximately 90°C.
8. This value determined from sample failure population, starting \( T_J = 25°C \), \( L = 0.15mH \), \( R_G = 50Ω, I_{AS} = 100A, V_{GS} = 10V \).
### Dynamic @ $T_J = 25^\circ C$ (unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{fs}$</td>
<td>Forward Transconductance</td>
<td>150</td>
<td>——</td>
<td>——</td>
<td>S</td>
<td>$V_{DS} = 10V$, $I_D = 100A$</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>Total Gate Charge</td>
<td>——</td>
<td>300</td>
<td>460</td>
<td>nC</td>
<td>$I_D = 100A$, $V_{DS} = 20V$</td>
</tr>
<tr>
<td>$Q_{gs}$</td>
<td>Gate-to-Source Charge</td>
<td>——</td>
<td>77</td>
<td>——</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>Gate-to-Drain (&quot;Miller&quot;) Charge</td>
<td>——</td>
<td>98</td>
<td>——</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{sync}$</td>
<td>Total Gate Charge Sync. ($Q_g - Q_{gd}$)</td>
<td>——</td>
<td>202</td>
<td>——</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{on}$</td>
<td>Turn-On Delay Time</td>
<td>——</td>
<td>32</td>
<td>——</td>
<td>ns</td>
<td>$V_{DD} = 20V$, $I_D = 100A$, $V_{GS} = 10V$</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise Time</td>
<td>——</td>
<td>105</td>
<td>——</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Turn-Off Delay Time</td>
<td>——</td>
<td>160</td>
<td>——</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall Time</td>
<td>——</td>
<td>100</td>
<td>——</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{iss}$</td>
<td>Input Capacitance</td>
<td>——</td>
<td>14240</td>
<td>——</td>
<td>pF</td>
<td>$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0 MHz$</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>Output Capacitance</td>
<td>——</td>
<td>2130</td>
<td>——</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{rss}$</td>
<td>Reverse Transfer Capacitance</td>
<td>——</td>
<td>1460</td>
<td>——</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{oss eff. (ER)}$</td>
<td>Effective Output Capacitance (Energy Related)</td>
<td>——</td>
<td>2605</td>
<td>——</td>
<td></td>
<td>$V_{GS} = 0V$, $V_{DS} = 0V$ to $32V$</td>
</tr>
<tr>
<td>$C_{oss eff. (TR)}$</td>
<td>Effective Output Capacitance (Time Related)</td>
<td>——</td>
<td>2920</td>
<td>——</td>
<td></td>
<td>$V_{GS} = 0V$, $V_{DS} = 0V$ to $32V$</td>
</tr>
</tbody>
</table>

### Diode Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_s$</td>
<td>Continuous Source Current (Body Diode)</td>
<td>——</td>
<td>——</td>
<td>394©</td>
<td>A</td>
<td>$V_{DD} = 20V$, $I_D = 100A$, $V_{DS} = 25V$, $V_{GS} = 0V$</td>
</tr>
<tr>
<td>$I_{SM}$</td>
<td>Pulsed Source Current (Body Diode)</td>
<td>——</td>
<td>——</td>
<td>1576</td>
<td>A</td>
<td>$V_{DD} = 20V$, $I_D = 100A$, $V_{DS} = 40V$</td>
</tr>
<tr>
<td>$V_{SD}$</td>
<td>Diode Forward Voltage</td>
<td>——</td>
<td>0.86</td>
<td>1.2</td>
<td>V</td>
<td>$T_J = 25^\circ C$, $I_S = 100A$, $V_{GS} = 0V$</td>
</tr>
<tr>
<td>$dV/dt$</td>
<td>Peak Diode Recovery ©</td>
<td>——</td>
<td>2.7</td>
<td>——</td>
<td>V/ns</td>
<td>$T_J = 175^\circ C$, $I_S = 100A$, $V_{DS} = 40V$</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Reverse Recovery Time</td>
<td>——</td>
<td>52</td>
<td>——</td>
<td>ns</td>
<td>$T_J = 25^\circ C$, $V_R = 34V$, $V_{GS} = 0V$</td>
</tr>
<tr>
<td>$Q_{tr}$</td>
<td>Reverse Recovery Charge</td>
<td>——</td>
<td>97</td>
<td>——</td>
<td>nC</td>
<td>$T_J = 25^\circ C$, $V_R = 34V$, $V_{GS} = 0V$, $di/dt = 100A/\mu s$</td>
</tr>
<tr>
<td>$I_{RPM}$</td>
<td>Reverse Recovery Current</td>
<td>——</td>
<td>2.3</td>
<td>——</td>
<td>A</td>
<td>$T_J = 25^\circ C$, $V_R = 34V$, $V_{GS} = 0V$</td>
</tr>
<tr>
<td>$t_{on}$</td>
<td>Forward Turn-On Time</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>A</td>
<td>Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)</td>
</tr>
</tbody>
</table>

MOSFET symbol showing the integral reverse p-n junction diode.
**Fig 3.** Typical Output Characteristics

**Fig 5.** Typical Transfer Characteristics

**Fig 6.** Normalized On-Resistance vs. Temperature

**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage
**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical COSS Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current
Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   - Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{j_{\text{max}}}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{j_{\text{max}}}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_D(\text{ave}) = \text{Average power dissipation per single avalanche pulse.}$
5. $BV = \text{Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).}$
6. $I_{av} = \text{Allowable avalanche current.}$
7. $\Delta T = \text{Allowable rise in junction temperature, not to exceed } T_{j_{\text{max}}} (\text{assumed as } 25^\circ \text{C in Figure 14, 15}).$
8. $t_{av} = \text{Average time in avalanche.}$
9. $D = \text{Duty cycle in avalanche} = t_{av} / t_2$
10. $Z_{thJC}(D, t_{av}) = \text{Transient thermal resistance, see Figures 13)}$

$$P_D(\text{ave}) = \frac{1}{2} (1.3 \cdot BV \cdot I_{av}) = \frac{\Delta T}{Z_{thJC}}$$
$$I_{av} = 2 \cdot \Delta T / (1.3 \cdot BV \cdot Z_{thJC})$$
$$E_{AS(AR)} = P_D(\text{ave}) \cdot I_{av}$$
Fig 17. Threshold Voltage vs. Temperature

Fig 18 - Typical Recovery Current vs. di/dt

Fig 19 - Typical Recovery Current vs. di/dt

Fig 20 - Typical Stored Charge vs. di/dt

Fig 21 - Typical Stored Charge vs. di/dt
Fig 22. Peak Diode Recovery \( \frac{dv}{dt} \) Test Circuit for N-Channel HEXFET® Power MOSFETs

**Fig 22a. Unclamped Inductive Test Circuit**

**Fig 22b. Unclamped Inductive Waveforms**

**Fig 23a. Switching Time Test Circuit**

**Fig 23b. Switching Time Waveforms**

**Fig 24a. Gate Charge Test Circuit**

**Fig 24b. Gate Charge Waveform**
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1769
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: *P" in assembly line position indicates "Lead-Free"

TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification information†

<table>
<thead>
<tr>
<th>Qualification level</th>
<th>Industrial†† (per JEDEC JESD47F††† guidelines)</th>
<th>TO-220</th>
<th>Not applicable</th>
</tr>
</thead>
<tbody>
<tr>
<td>RoHS compliant</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

† Qualification standards can be found at International Rectifier’s web site: http://www.irf.com/product-info/reliability/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/who-to-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.